

**Abstract****Logic basic cell, logic basic cell array and logic device**

5 A logic basic cell contains a first logic function block and a second logic function block for the logic combination of a first input signal and a second input signal in accordance with a predetermined first or second logic subfunction, and a first logic transistor coupled to the first logic function

10 block, having a gate terminal, at which a third input signal can be provided, and having a source/drain terminal at which the output signal can be provided. Furthermore, a second logic transistor coupled to the second logic function block is provided, having a gate terminal, at which a complementary

15 signal with respect to the third input signal can be provided, and having a source/drain terminal, which is coupled to the source/drain terminal of the first logic transistor.

**List of reference symbols**

- 100 Logic basic cell
- 101 First data signal path
- 5 101a First n-MOS partial path
- 101b Second n-MOS partial path
- 102 Second data signal path
- 102a First p-MOS partial path
- 102b Second p-MOS partial path
- 10 103 First data signal input
- 104 Second data signal input
- 105 Third data signal input
- 106 Fourth data signal input
- 107a Data signal output
- 15 107b Data signal output
- 108 First n-MOS logic selection transistor
- 109 Second n-MOS logic selection transistor
- 110 Third n-MOS logic selection transistor
- 111 Fourth n-MOS logic selection transistor
- 20 112 First n-MOS data signal transistor
- 113 Second n-MOS data signal transistor
- 114 Third n-MOS data signal transistor
- 115 Fourth n-MOS data signal transistor
- 116 First p-MOS logic selection transistor
- 25 117 Second p-MOS logic selection transistor
- 118 Third p-MOS logic selection transistor
- 119 Fourth p-MOS logic selection transistor
- 120 First p-MOS data signal transistor
- 121 Second p-MOS data signal transistor
- 30 122 Third p-MOS data signal transistor
- 123 Fourth p-MOS data signal transistor
- 124 First inverter
- 125 Second inverter
- 126 Ground potential
- 35 127 Supply potential

128 Third inverter  
129 First n-MOS logic transistor  
130 Second n-MOS logic transistor  
131 First p-MOS logic transistor  
5 132 Second p-MOS logic transistor  
140 First logic function block  
150 Second logic function block  
160 First logic function block  
170 Second logic function block  
10 200 Table  
300 Logic function block  
301 First inverter circuit  
302 First n-MOS inverter transistor  
303 First p-MOS inverter transistor  
15 304 Second inverter circuit  
305 Second n-MOS inverter transistor  
306 Second p-MOS inverter transistor  
307 Supply potential  
308 Ground potential  
20 309 Signal path unit  
310 First signal path input  
311 Second signal path input  
312 Third signal path input  
313 Fourth signal path input  
25 314 First p-MOS logic transistor  
315 Second p-MOS logic transistor  
316 Third p-MOS logic transistor  
317 Fourth p-MOS logic transistor  
318 Fifth p-MOS logic transistor  
30 319 Sixth p-MOS logic transistor  
320 Seventh p-MOS logic transistor  
321 Eighth p-MOS logic transistor  
322 Ninth p-MOS logic transistor  
323 Tenth p-MOS logic transistor  
35 324 Eleventh p-MOS logic transistor